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# A SINGLE LAYER WIRING BOND PAD WITH OPTIMUM AL FILM THICKNESS IN CU/FSG PROCESS FOR DEVICES UNDER PADS

## TECHNICAL FIELD

001 The present invention relates to methods and apparatus for the testing of semiconductor devices. The present invention also relates to microelectronic devices and methods of fabrication therefore, and more particularly, to bonding pad structures for microelectronic devices and methods of fabrication therefore.

## BACKGROUND OF THE INVENTION

002 In the fabrication processes for semiconductor devices, an integrated circuit (IC) chip is frequently assembled in a package in a final process step to complete the fabrication process. The assembled package can then be connected to a printed circuit board as part of a large circuit. To establish an electrical communication with the integrated circuit chip, a wire bonding process is frequently utilized to connect a multiplicity of bond pads on the integrated circuit chip to the outside circuitry.

003 In a typical IC chip, for example, active circuit elements such as transistors, resistors, etc., can be positioned in a central portion, i.e., the active region, of the chip while

the bond pads are normally arranged around the periphery of the active region such that active circuit elements are not likely to be damaged during a subsequent bonding process. When a wire bonding process is performed on a bond pad on an IC chip, the process normally entails the bonding of a gold or aluminum wire to the bond pad by fusing the two together with ultrasonic energy. The wire is then pulled away from the bond pad after the bond is formed. During the pulling of the gold wire from the bond, a defect known as bond pad lift-off is frequently encountered. It occurs based on the fact that during the attaching process of a gold wire to a bond pad, a high level of stress is placed on the bond pad. It occurs because a relatively large, heavy bond is placed on top of layers, which may not have strong adhesion to the underlying layers.

004 Bonding pads (also referred to as "bond pads") in microelectronic devices such as integrated circuits are commonly used during electric die sort (EDS) tests and other testing and fabrication processes. A typical bonding pad includes a plurality of metal wiring layers, connected to each other by a contact plug. The bonding pad typically has relatively low conductivity because the contact plug that connects the metal wiring layers is typically made of tungsten.

005 When a probe tip is connected to a bonding pad during a process such as EDS, physical force may be applied to the bonding pad to the point that damage to the bonding pad

structure may occur. Similarly, wire-bonding processes may apply sufficient force to the bonding pad such that the structure of the bonding pad is damaged.

006 After an integrated circuit is fabricated, external connections must be formed before the chip is embedded in plastic for protection. With aluminum wiring, which has been the standard for many years, the upper level of wiring for the chip would include bond pads with necessary connections to the underlying circuit. After the protective overcoat (PO) layer is deposited over the chip, holes are etched through the PO to provide access to the bond pads. Depending on the type of packaging used, external connections from the chip can then be made by thin wires which are typically ultrasonically bonded to the bond pad, or by the formation of solder balls which make a direct connection between the bond pad on the chip and the external connector.

007 Traditional wiring bonds pads have been configured as fully layer structures. For example, traditional wiring bonds pads have been arranged as metal-1 to metal-8 structures in an eight-layer metal process. Current wiring pad design rules do not permit only one layer for wiring bond configurations, due to wire bonding stress-reduced fractures that can result during packaging. Devices present under wiring pads have also been prohibited according to traditional wiring bond pad rules.

## BRIEF SUMMARY OF THE INVENTION

008 The following summary of the invention is provided to facilitate an understanding of some of the innovative features unique to the present invention, and is not intended to be a full description. A full appreciation of the various aspects of the invention can be gained by taking the entire specification, claims, drawings, and abstract as a whole.

009 It is therefore one aspect of the present invention to provide a method for forming a wiring bond pad that can be utilized in wire bonding operations on an integrated circuit device.

0010 It is another aspect of the present invention to provide an improved wiring bond pad apparatus.

0011 It is still another aspect of the present invention to provide a wiring bond pad formed from a single metal layer.

0012 It is yet another aspect of the present invention to reduce chip size and improve bond pad efficiency by providing a wiring bond pad formed from a single metal layer located above a plurality of intermetal dielectric (IMD) layers.

0013 It is an additional aspect of the present invention to provide a layer of aluminum film formed above a single metal layer of copper, wherein the single metal layer of copper is

configured to comprise a wiring bond pad and the layer of aluminum film comprises an optical film thickness to avoid damage that can occur from wiring bonding processes and operations thereof.

0014 The above and other aspects of the present invention can thus be achieved as is now described. A method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit device is disclosed herein, including a wiring bond apparatus thereof. A wiring bond pad may be configured to comprise a single metal layer. At least one integrated circuit device may be positioned below the wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad as a single metal layer wiring bond pad. The wiring bond pad may thus be configured as a single metal layer wiring bond pad. The single metal layer is generally located above a plurality of intermetal dielectric layers.

0015 The integrated circuit device may also be located below the plurality of intermetal dielectric layers. The single metal layer may comprise a metal-8 layer. The plurality of intermetal dielectric layers can be configured to comprise IMD-1 to IMD-7 layers. The metal-8 layer may comprise a copper layer. A layer of aluminum film may be formed above the single metal layer. The aluminum film formed above the single metal layer can comprise a layer having a thickness in a range of and including 10KÅ to

20KÅ. The single metal layer may also comprise a copper layer having a thickness of approximately 10KÅ. The aluminum film located above the single metal layer may thus comprise a buffer and bonding layer.

## BRIEF DESCRIPTION OF THE DRAWINGS

0016 The accompanying figures, in which like reference numerals refer to identical or functionally-similar elements throughout the separate views and which are incorporated in and form part of the specification, further illustrate the present invention and, together with the detailed description of the invention, serve to explain the principles of the present invention.

0017 FIG. 1 illustrates a block diagram of a single layer bond pad and an associated layer of aluminum film, including a plurality of intermetal dielectric (IMD) layers thereof, in accordance with a preferred embodiment of the present invention;

0018 FIG. 2 depicts a block diagram of a prior art conventional wiring bond pad;

0019 FIG. 3 illustrates a cross-sectional view of a single layer Cu metal-8 bond pad after an AL wedge wiring bond, in accordance with a preferred embodiment of the present invention;

0020 FIG. 4 depicts a configuration illustrating thicker aluminum bond pad effects, in accordance with a preferred embodiment of the present invention; and

0021 FIG. 5 illustrates a graph illustrating aluminum pad thickness and material properties, in accordance with a preferred embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

0022 The particular values and configurations discussed in these non-limiting examples can be varied and are cited merely to illustrate embodiments of the present invention and are not intended to limit the scope of the invention.

0023 FIG. 1 illustrates a block diagram of a single layer bond pad and an associated layer of aluminum film, including a plurality of intermetal dielectric (IMD) layers thereof, in accordance with a preferred embodiment of the present invention. The configuration depicted in FIG. 1 is ideally suited for forming a single layer wiring bond pad with optimum aluminum film thickness in copper/FSG processes for integrated circuit devices "under" wiring bond pads. Note that as utilized herein, the term "FSG" generally refers to "fluorinated silica glass". FSG is typically employed as a low dielectric constant (low-k) material for intermetal dielectric (IMD) layers for semiconductor technology of extremely small sizes.

0024 The single layer bond pad can be formed from a single metal layer 12, as indicated in FIG. 1. Single metal layer 12 may be formed from copper and may comprise a metal-8 (i.e. M8) wiring bond pad. Single metal layer 12 may possess a thickness of approximately 10KÅ. A layer 14 of aluminum film is generally positioned above single metal layer 12.

0025 Layer 14 may be configured as a layer of aluminum film possessing a thickness in a range of approximately 10KÅ to 20KÅ. Layer 14 thus functions as a buffer and bonding layer, when positioned above single metal layer 12 (i.e. single layer M8 bond pad). Bonding mechanical stresses are illustrated by arrow 12, which also indicates the general direction of an associated wiring bond. Additionally, a plurality of intermetal dielectric (IMD) layers 18 is generally illustrated in FIG. 1 to include IMD1 to IMD7 metal layers. A device 20, such as, for example, an integrated circuit device, may be positioned below layers IMD1 to IMD7 to comprise a device under a single layer bond pad.

0026 FIG. 2 depicts a block diagram of a prior art conventional wiring bond pad 24. Bond pad 24 is indicated in FIG. 2 to illustrate the fact that traditional wiring bond pads are generally full layer structures. For example, in FIG. 2, metal-1 (M1) to metal-8 (M1) layers are indicated. An M1 layer 42 thus is positioned below an M2 layer 40, while an M3 layer 38 is located below an M4 layer 36. An M5 layer 34 is positioned below an M6 layer 32, while an M7 layer 30 is positioned below an

M8 layer 28. Traditional wiring bond pad design rules, generally do not permit only one metal layer to be utilized for implementing a wiring bond pad due to wiring bond stress-induced fracture during packaging. Bonding mechanical stresses are indicated in FIG. 2 by arrow 26, which also illustrates the general direction of such bonding mechanical stresses.

0027 Additionally IMD1 to IMD 7 layers are illustrated, as indicated by arrows 46. An interlayer dielectric (ILD) is indicated by arrow 44. Via-1 to Via 7 are also depicted in FIG. 2. It is thus apparent that a major difference between the configurations of FIG. 1 and FIG. 2 lies in the ability of the design illustrated in FIG. 1 to form a wiring bond pad from a single metal layer, without experiencing stress-induced fractures. The design depicted in FIG. 2 will suffer from stress-induced fractures, if an attempt is made to implement a single metal layer as a wiring bond pad.

0028 FIG. 3 illustrates a cross-sectional view 60 of a single layer Cu metal-8 bond pad after an AL wedge wiring bond, in accordance with a preferred embodiment of the present invention. Active devices are generally positioned under the single layer Cu metal-8 bond pad. The configuration illustrated in FIG. 3 thus includes a buffer 62, positioned above a single layer Cu metal-8 (M8) bond pad 64. A plurality of IMD layers 66 are also indicated. Layers 66 of FIG. 3 are analogous to IMD1 to IMD 7 layers 18 of FIG. 1.

0029 FIG. 4 depicts a configuration illustrating thicker aluminum bond pad effects, in accordance with a preferred embodiment of the present invention. All of the associated stresses are generally decreased as the aluminum thickness is increased. Thus, by increasing the aluminum thickness, an enhanced buffer layer can be created to protect the "under" IMD layer from damage that may result from ultrasonic motion. In FIG. 14, a configuration 70 is illustrated indicated a control thickness of 12K resulting from the formation of an aluminum buffer layer 72. Such a layer 72 thus possesses a layer thickness of approximately 12KÅ. A copper wiring bond pad 74 is formed from a single copper metal layer. An aluminum bond pad 76 is also illustrated via configuration 70. Similarly, configuration 71 includes an aluminum bond pad 86 positioned above an aluminum buffer layer 82, which possesses a thickness of approximately 16KÅ. A copper wiring bond pad 84 is also indicated in configuration 71.

0030 FIG. 5 illustrates a graph 90 illustrating aluminum pad thickness and material properties, in accordance with a preferred embodiment of the present invention. Note that in graph 90 of FIG. 5, reference numeral 92 is associated with configuration 70 of FIG. 4, while reference numeral 94 is associated with configuration 71 of FIG. 4. FIG. 5 illustrates the fact that the aluminum bond pad thickness and material property can protect the IMD layers and associated silicon crater, which may occur during formation of the bond pad and/or associated integrated circuit

devices and components. The following variables generally indicated the high-level stress functions indicated in FIG. 5:

$S_x$ = normal stress

$S_z$ = shear stress

$S_1$ = tensile stress

$S_{xz}$ = angular shear stress

$S_{equ}$ = total equivalent stress

0031 It can thus be appreciated, based on the foregoing description that a method is disclosed herein for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit device is disclosed herein. An improved wiring bond apparatus is also disclosed herein. According to this method and apparatus thereof, a wiring bond pad may be configured to comprise a single metal layer. At least one integrated circuit device may be positioned below the wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad as a single metal layer wiring bond pad. The wiring bond pad may thus be configured as a single metal layer wiring bond pad. The single metal layer is generally located above a plurality of intermetal dielectric layers.

0032 The integrated circuit device may also be located below the plurality of intermetal dielectric layers. The single metal layer may comprise a metal-8 layer. The plurality of intermetal

dielectric layers can be configured to comprise IMD-1 to IMD-7 layers. The metal-8 layer may comprise a copper layer. A layer of aluminum film may be formed above the single metal layer. The aluminum film formed above the single metal layer can comprise a layer having a thickness in a range of and including 10KÅ to 20KÅ. The single metal layer may also comprise a copper layer having a thickness of approximately 10KÅ. The aluminum film located above the single metal layer may thus comprise a buffer and bonding layer.

0033 The embodiments and examples set forth herein are presented to best explain the present invention and its practical application and to thereby enable those skilled in the art to make and utilize the invention. Those skilled in the art, however, will recognize that the foregoing description and examples have been presented for the purpose of illustration and example only. Other variations and modifications of the present invention will be apparent to those of skill in the art, and it is the intent of the appended claims that such variations and modifications be covered. The description as set forth is thus not intended to be exhaustive or to limit the scope of the invention. Many modifications and variations are possible in light of the above teaching without departing from scope of the following claims. It is contemplated that the use of the present invention can involve components having different characteristics. It is intended that the scope of the present invention be defined

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by the claims appended hereto, giving full cognizance to equivalents in all respects.